CLAIMS

1. A method for use in designing a reticle for exposing a substrate during production of a circuit, comprising:

determining the relative isolation of first type features to be produced using the reticle with respect to adjacent features;

sizing first type apertures in the reticle corresponding to the first type features using different sizing rules depending on the relative isolation of the first type features;

determining dimensions of second type features to be produced using the same reticle; and

sizing second type apertures corresponding to the second type features in the same reticle using different sizing rules depending on the dimensions of the second type features.

2. A method according to claim 1, wherein the results of the relative isolation determining step cause the more isolated first type apertures to be made larger.

3. A method according to claim 1 or 2, wherein the relative isolation is determined against a first threshold, with the more isolated first type apertures being sized a first way and the less isolated first type apertures sized a second way.

4. A method according to any one of the preceding claims, further comprising the step of extending the size of at least some of the second type apertures in a second dimension orthogonal to a first dimension.

5. A method according to any one of the preceding claims, wherein the results of the first dimension determining step cause the second dimension of the smaller second type apertures to be made larger.

6. A method according to any one of the preceding claims, wherein the first type features comprises a plurality of holes.

7. A method according to any one of the preceding claims, wherein the second type features comprises a plurality of slits.

8. A method according to any one of the preceding claims, wherein the results of the first dimension determining step cause the second type apertures to be sized in the second dimension, orthogonal to the first dimension.

9. A method according to any one of the preceding claims, wherein the second type apertures corresponding to the second type features with the smaller first dimension are increased in the second dimension more than those with the larger first dimension.

10. A method according to any one of the preceding claims, wherein the first dimension is compared with a second threshold, with the larger second type apertures being sized a third way and the smaller second type apertures sized a fourth way.

11. A method according to any one of the preceding claims, wherein the first dimension of a feature is the length of the feature.

12. A method according to any one of the preceding claims, wherein the features are features of memory cells.

13. A method according to any one of the preceding claims, wherein the reticle is a Half-Tone Phase Shift Mask.

14. A method according to any one of the preceding claims for producing features for a local interconnect layer.

15. A reticle for exposing a substrate during production of a circuit, comprising:

a plurality of first type apertures sized using different sizing rules depending on the relative isolation of first type features of the circuit corresponding to the first type apertures; and

a plurality of second type apertures sized using different sizing rules depending on the dimensions of second type features of the circuit corresponding to the second type apertures.

16. A reticle according to claim 15, wherein the more isolated first type apertures are relatively larger than the less isolated first type apertures corresponding to the size of features to be produced.

17. A reticle according to claim 15 or 16, wherein the first type apertures are apertures for producing holes.

18. A reticle according to any one of claims 15 to 17, wherein the second type apertures are apertures for producing slits.

19. A reticle according to any one of claims 15 to 18, wherein the size in a first dimension determines size in a second dimension, orthogonal to the first dimension.

20. A reticle according to any one of claims 15 to 19, wherein the second type features determined to be small in the first dimension are larger in the second dimension than those determined to be the larger in the first dimension.

21. A reticle according to any one of claims 15 to 20, wherein larger and smaller in the first dimension is determined by comparison with a threshold.

22. A reticle according to any one of claims 15 to 21, wherein the first dimension of a feature is the length of the feature.

23. A reticle according to any one of claims 15 to 22, wherein the features are features of memory cells.

24. A reticle according to any one of claims 15 to 23, wherein the reticle is a Half-Tone Phase Shift Mask.

25. A reticle according to any one of claims 15 to 24, being a local interconnect layer reticle.

26. A reticle designed according to the method of any one of claims 1 to 14.

27. A reticle according to any one of claims 15 to 25, designed according to the method of any one of claims 1 to 14.

28. A method of producing an integrated circuit comprising the steps of:
designing a reticle in accordance with the method of any one of claims 1 to 14;
producing the so designed reticle; and
using said reticle to expose features of both the first and second types in a single step in at least one layer of at least a portion of the integrated circuit.

29. A method of producing an integrated circuit comprising using a reticle as defined in any one of claims 15 to 27 to print features of both the first and second types in a single step in at least a portion of the integrated circuit.

30. An integrated circuit, at least a portion of which is produced using a reticle as defined in any one of claims 15 to 27.